1. Convert $4096_{10}$, $-2,047_{10}$, and $-2,000,000_{10}$ into 32-bit two’s complement binary numbers, respectively, and convert the following two’s complement binary numbers to be decimal numbers:
   
   a. 1111 1111 1111 1111 1111 1111 0000 0110$_{two}$;
   b. 1111 1111 1111 1111 1111 1111 1110 1111$_{two}$;
   c. 0111 1111 1111 1111 1111 1111 1110 1111$_{two}$.

2. Suppose that all of the conditional branch instructions except beq and bne were removed from the MIPS instruction set along with slt and all of its variants (slti, sltu, sltui). Show how to perform

   \[
   \text{slt} \quad $t0, $s0, $s1
   \]

   using the modified instruction set in which slt is not available. (Hint: It requires more than two instructions.)

3. Show the IEEE 754 binary representation for the floating-point numbers $10_{ten}$, $10.5_{ten}$, $0.1_{ten}$, and $-2/3$, respectively.

4. With $x = 0000 0000 0000 0000 0000 0000 0101 1011$_{two}$ and $y = 0000 0000 0000 0000 0000 0000 0000 1101$_{two}$ representing two’s complement signed integers, perform, showing all work:
   
   a. $x+y$
   b. $x-y$
   c. $x*y$
   d. $x/y$