Digital System Design for Circuit and Electronics

Additional material

Intro. VLSI: CMOS inverter

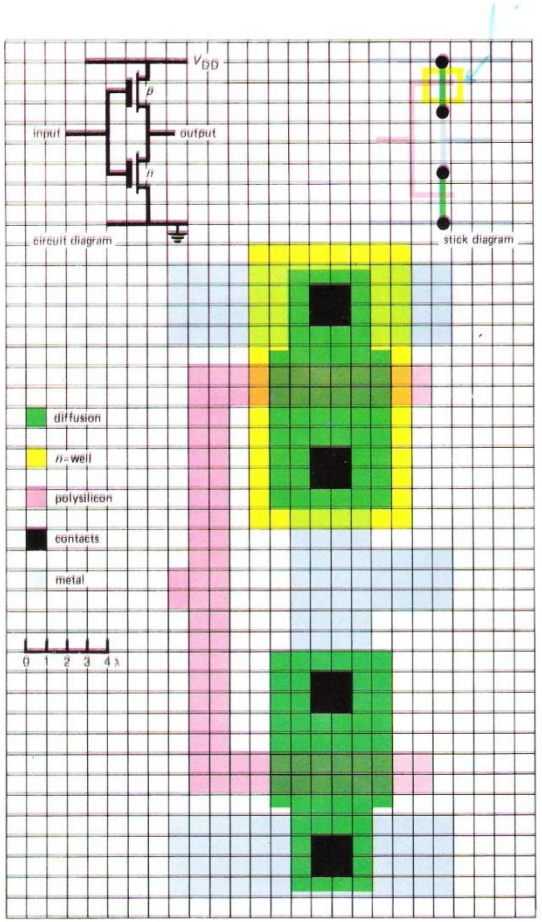
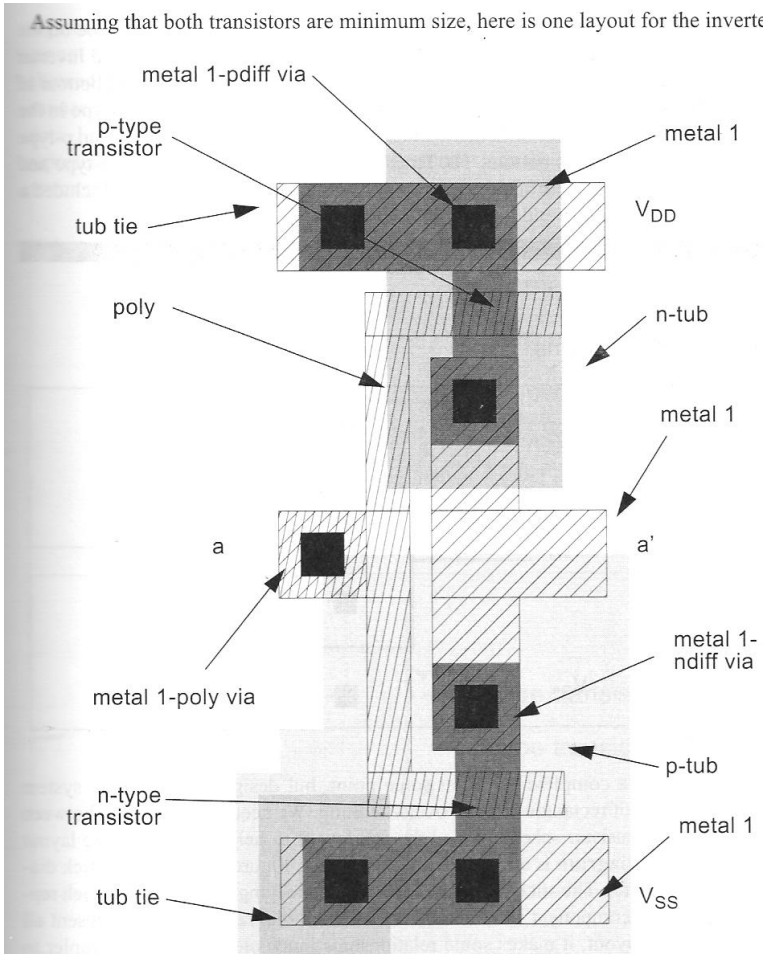


Plate 5 Layout of simple CMOS inverter (version of Fig. 3.12).

CMOS inverter: black and white representation



A counter layout

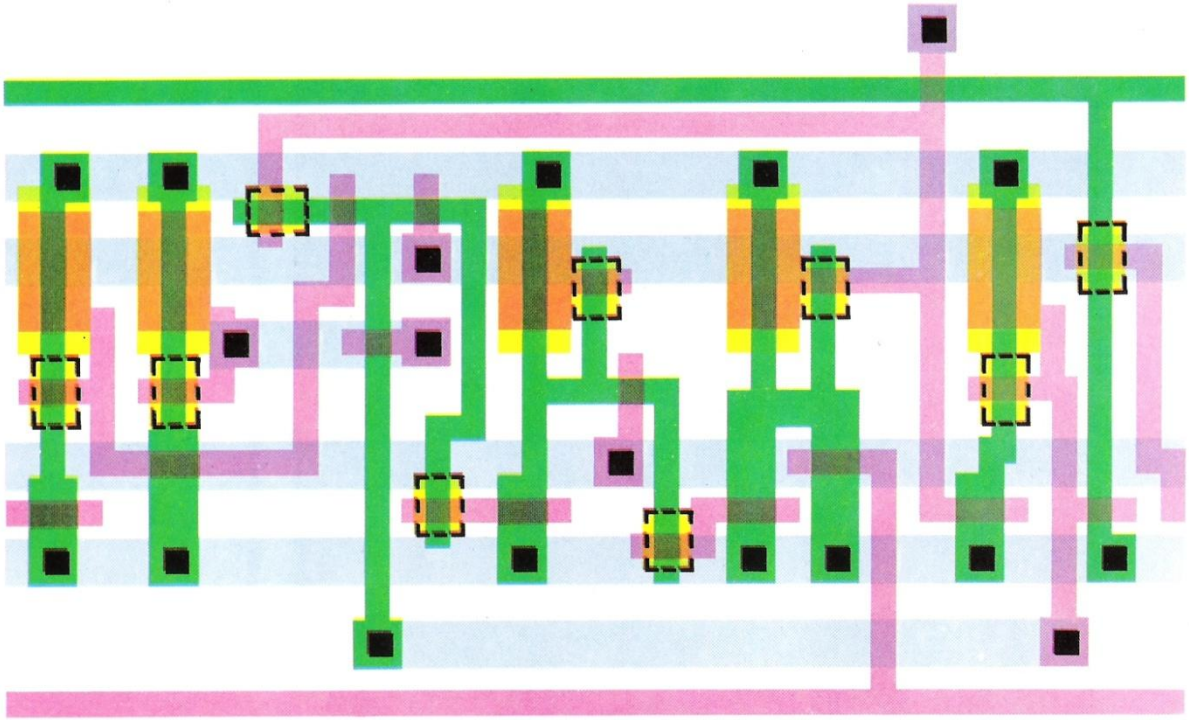


Plate 10 Completed layout for counter example of Appendix A (version of Fig. A.6).

Rules for design rule checking: basic rules

metal 1 Minimum width is 3 λ, minimum separation is 3 λ.

metal 2 Minimum width is 3 λ, minimum separation is 4 λ.

polysilicon Minimum width is 2 λ, minimum poly–poly separation is 2 λ.

p-, n-diffusion Minimum width is 3 λ, minimum separation between same-type diffusions is 3 λ, minimum p-diff–n-diff separation is 10 λ.

tubs Tubs must be at least 10 λ wide. The minimum distance from the tub edge to source/drain active area is 5 λ.

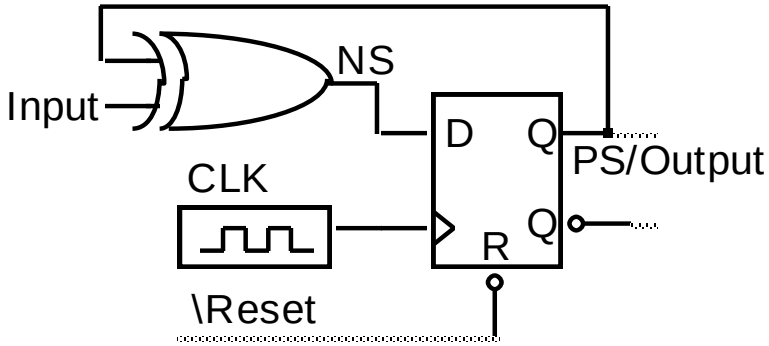
Rules for composition

- **transistors** The smallest transistor is of width 3 λ and length 2 λ; poly extends 2 λ beyond the active region and diffusion extends 3 λ. The active region must be at least 1 λ from a poly-metal via, 2 λ from another transistor, and 3 λ from a tub tie.
- **vias** Cuts are 2 λ × 2 λ: the material on both layers to be connected extends 1 λ in all directions from the cut, making the total via size 4 λ × 4 λ. (MOSIS also suggests another via construction with 1.5 λ of material around the cut. This construction is safer but the fractional design rule may cause problems with some design tools.) Available via types are:
  - n/p-diffusion–poly;
  - poly–metal 1;
  - n/p-diffusion–metal 1;
  - metal 1–metal 2;

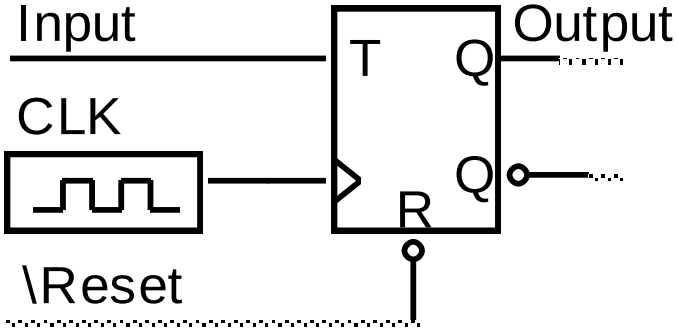
Concept of the State Machine
Example: Odd Parity Checker

Next State/Output Functions

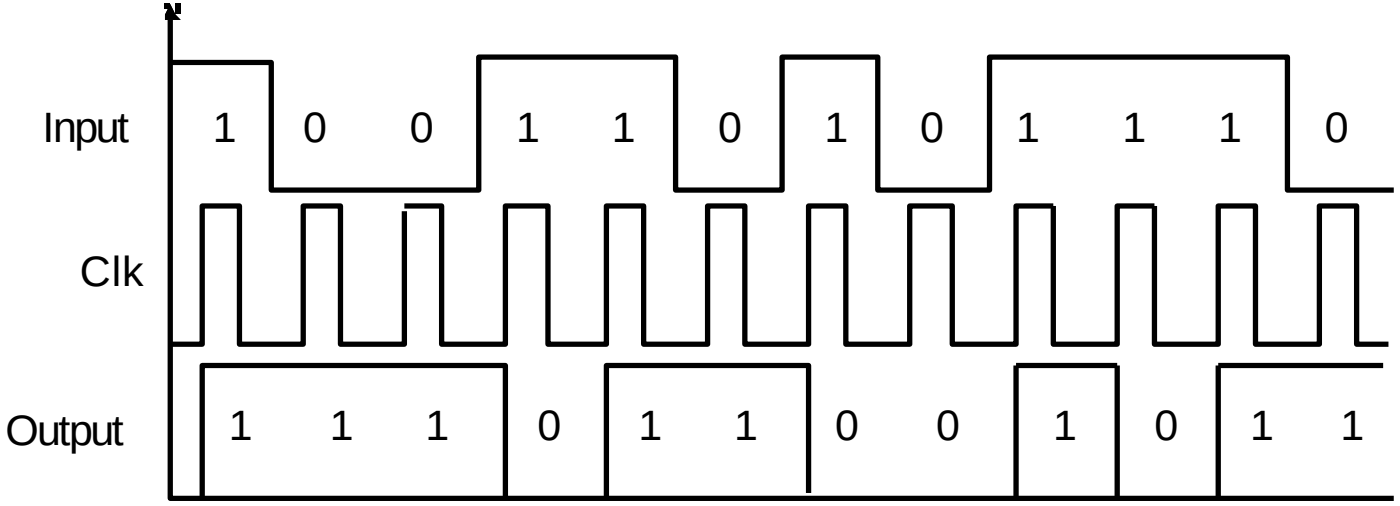
NS = PS xor PI; OUT = PS



D FF Implementation



T FF Implementation



Timing Behavior: Input 1 0 0 1 1 0 1 0 1 1 1 0

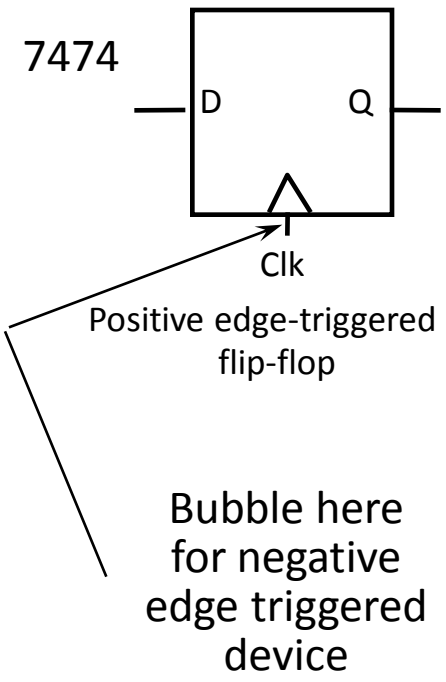
State Behavior of R-S Latch

S	R	Q
0	0	hold
0	1	0
1	0	1
1	1	unstable

Truth Table Summary
of R-S Latch Behavior

D-FlipFlop

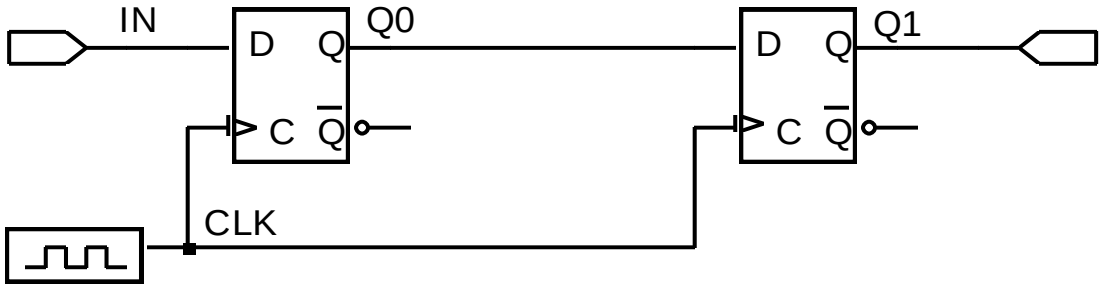
Edge triggered device sample inputs on the event edge



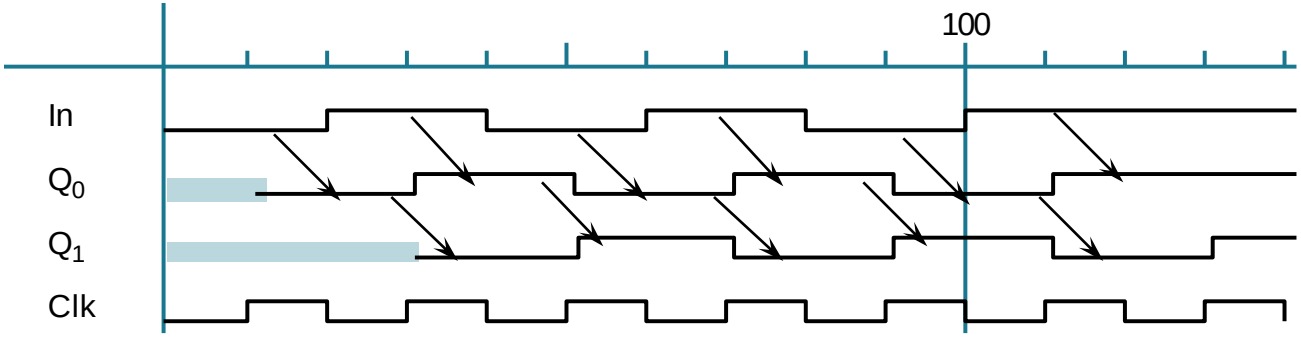
Cascaded Flipflops and Setup/Hold/Propagation Delays

Shift Register
S,R are preset, preclear

New value to first stage while second stage obtains current value of first stage



Correct Operation, assuming positive edge triggered FF



Design Procedure

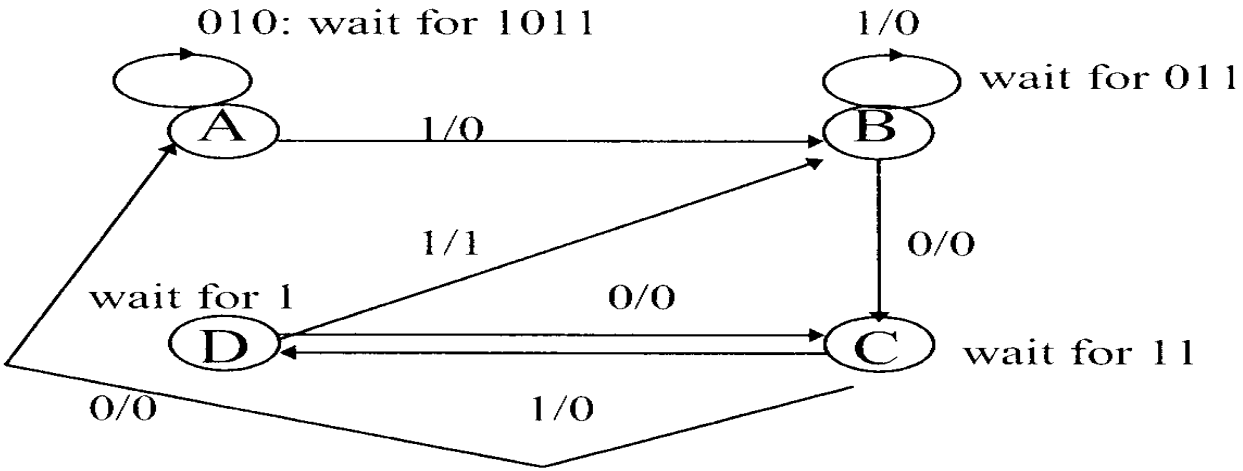
Excitation Tables: What are the necessary inputs to cause a particular kind of change in state?

Q	Q^+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Design problem

- Please design a sequence recognizer of

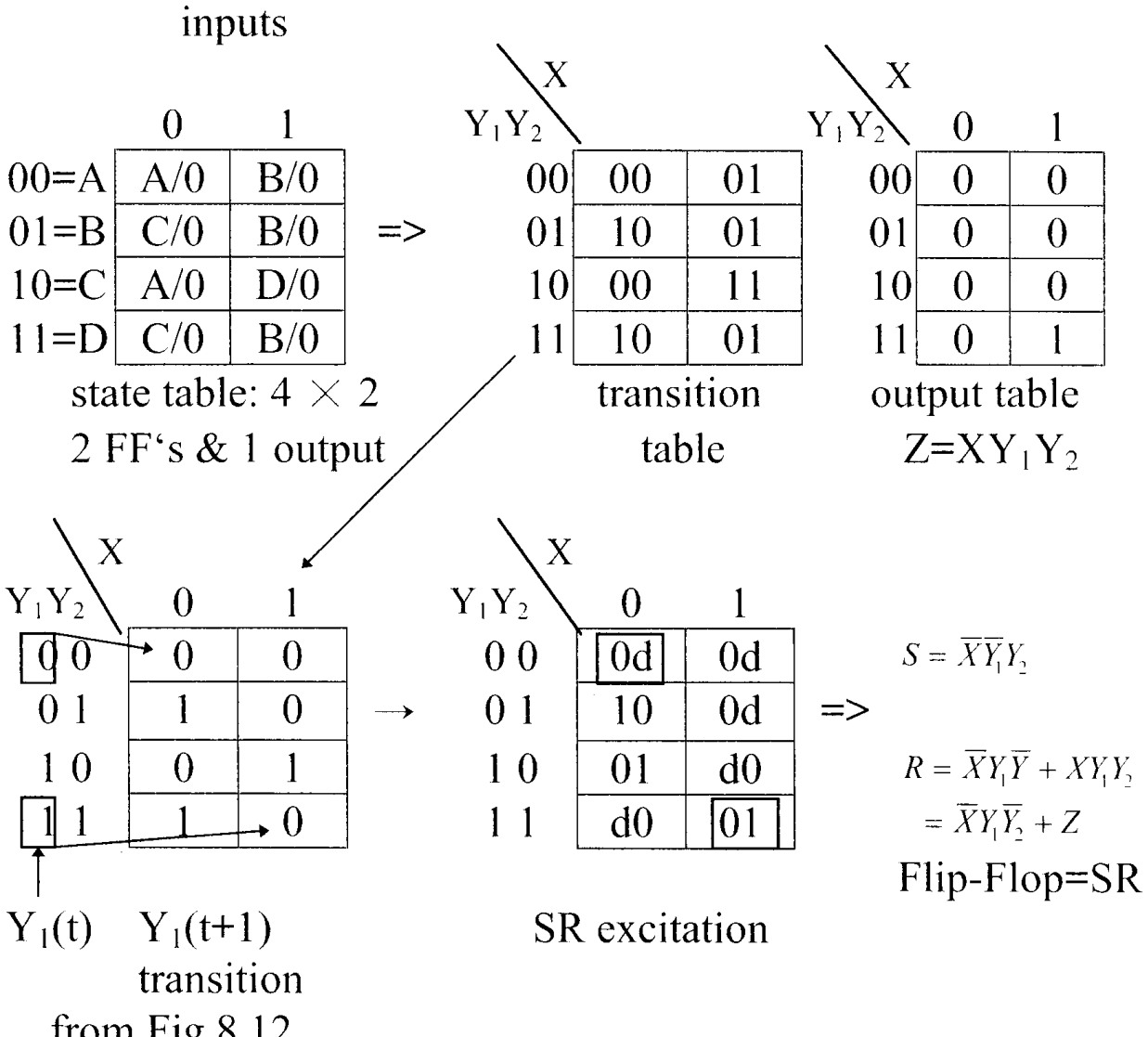
  1011, using first a RS flip-flop, then a D flip flop.



Ex.

Design a sequential circuit that detects an input sequence of 1011. The sequence may overlap.

A 1011 sequence defector gives an output of 1 when the input completes a sequence of 1011. Because overlap is allowed the last 1 in the 1011 sequence could be the first bit of the next 1011 sequence, and hence a further input of 011 is enough to produce an output of 1. That is, the input sequence 1011011 consists of two overlapping sequences.


inputs
0 1
00=A A/0 B/0
01=B C/0 B/0
10=C A/0 D/0
11=D C/0 B/0
state table: 4 × 2
2 FF's & 1 output
=>
X
Y1Y2
00 00 01
01 10 01
10 00 11
11 10 01
transition table
X
Y1Y2 0 1
00 0 0
01 0 0
10 0 0
11 0 1
output table
Z=XY1Y2
X
Y1Y2 0 1
0 0 0 0
0 1 1 0
1 0 0 1
1 1 1 0
Y1(t) Y1(t+1)
transition
from Fig.8.12
→
X
Y1Y2 0 1
0 0 0d 0d
0 1 10 0d
1 0 01 d0
1 1 d0 01
SR excitation
=>
S = X̄Y1Ȳ2
R = X̄Y1Ȳ + XY1Y2
= X̄Y1Ȳ2 + Z
Flip-Flop=SR

Results

X	0	1		
00 Y1 Y2	0	1		
01	0	1		
10	0	1		
11	0	1		

X	0	1		
00	0	1		
01	0	1		
10	0	1		
11	0	1		

Input = X

D = X

S = X'Y1' Y2

R = X'Y1Y2' + X Y1 Y2

Z = X Y1 Y2 (output)

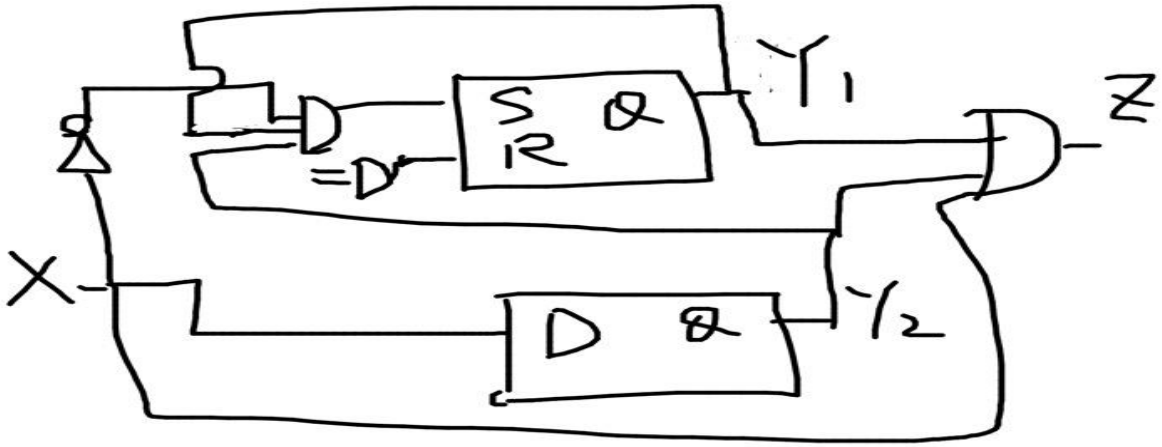
Circuit of 1011 recognizer

input = x

$D = X$, $S = X' Y_1' Y_2$

$R = X' Y_1 Y_2' + X Y_1 Y_2$

output $Z = X Y_1 Y_2$



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